Evaluation Board for the AD9831 Direct Digital Synthesizer

EVAL-AD9831EB

FEATURES
Full-Featured Evaluation Board for the AD9831
Various Linking Options
PC Software for Control of AD9831

INTRODUCTION

This Application Note describes the evaluation board for the AD9831 Direct Digital Synthesizer (DDS). The AD9831 is a numerically controlled oscillator employing a phase accumulator, a sine look-up table and a 10-bit D/A converter. The part can be operated with clock frequencies up to 25 MHz. Both phase modulation and frequency modulation can be performed with the AD9831. Full data on the AD9831 is available in the AD9831 datasheet available from Analog Devices and should be consulted in conjunction with this Application Note when using the evaluation board.

The evaluation board interfaces to the parallel port of an IBM compatible PC. Software is available with the evaluation board which allows the user to easily program the AD9831.

Components on the AD9831 Evaluation Board include a 25 MHz oscillator which provides the MCLK for the AD9831. The user can remove this oscillator, if required, and drive the AD9831 with a different clock oscillator or an external clock source via a BNC connector. Latches (74HC574) are also on the board, these latches being used to hold the 16-bit data word being written from the PC to the AD9831.

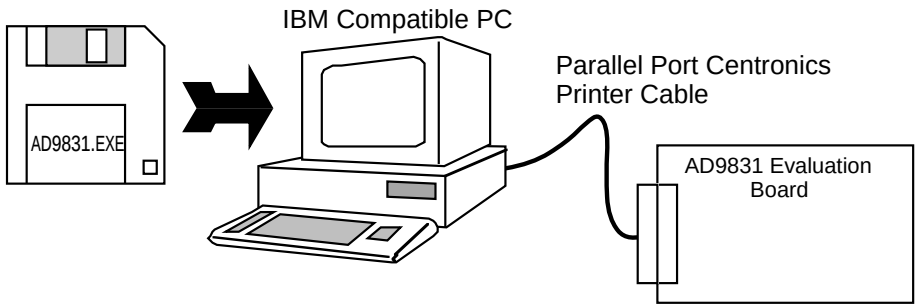
OPERATING THE AD9831 EVALUATION BOARD

Power Supplies

This evaluation board has two analog power supply inputs: AVDD and AGND. AVDD equals +5 V or +3.3 V and is used to provide the AVDD for the AD9831. DGND and DVDD connections are also available. The DVDD is used to provide the DVDD for the AD9831, the 25 MHz oscillator and the DVDD for the logic chips. DGND and AGND are connected at the AD9831. Therefore, it is recommended not to connect AGND and DGND elsewhere in the system.

All power supplies are decoupled to ground. AVDD and DVDD are decoupled using 10µF tantalum capacitors and 0.1µF ceramic capacitors at the input to the evaluation board. The power supplies are again decoupled using 0.1µF capacitors at the AD9831, the crystal and the logic.

Evaluation Board Setup



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REV O

Link and Switch Options

There are five link options which must be set for the required operating setup before using the evaluation board. The functions of these options are outlined below.

Link No.	Function
LK1	The PSEL1 input can be controlled by the user via a BNC connector or, alternatively, by switch SW.
	When LK1 is arranged so that PSEL1 is connected to SW, the user can control the PSEL1 signal using the double throw switch.
	Alternatively, PSEL1 can be tied to a BNC connector by altering LK1 so that the user can provide the PSEL1 control from a logic source.
LK2	The PSEL0 input can be controlled by the user via a BNC connector or, alternatively, by switch SW.
	When LK2 is arranged so that PSEL0 is connected to SW, the user can control the PSEL0 signal using the double throw switch.
	Alternatively, PSEL0 can be tied to a BNC connector by altering LK2 so that the user can provide the PSEL0 control from a logic source.
LK3	The FSELECT input can be controlled by the user via a BNC connector or, alternatively, by switch SW.
	When LK3 is arranged so that FSELECT is connected to SW, the user can control the FSELECT signal using the double throw switch.
	Alternatively, FSELECT can be tied to a BNC connector by altering LK3 so that the user can provide the FSELECT control from a logic source.
LK4	LK4 is used to place the AD9831 in sleep mode.
	When LK4 is connected so that $\overline{\text{SLEEP}}$ is tied to DGND, the AD9831 is placed in sleep mode whereby the AD9831's internal clocks, REFOUT and the DAC are disabled.
	When LK4 is connected so that $\overline{\text{SLEEP}}$ is tied to DVDD, the AD9831 is powered up.
LK5	The reference to the AD9831 can be provided by the on-board reference, which is available at REFOUT, or an external reference of nominal value 1.21 V can be used. When LK5 is closed, the on-board reference is used. When this link is opened, REFIN is disconnected from REFOUT and the reference can be provided by the user via a BNC connector.

SET-UP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as per the required operating mode. Table 1 shows the position in which all the links are set when the evaluation board is sent out.

Table 1. Initial Link and Switch Positions

Link No.	Function
LK1	LK1 is arranged so that PSEL1 is tied to SW.
LK2	LK2 is arranged so that PSEL0 is tied to SW.
LK3	LK3 is arranged so that FSELECT is tied to SW.
LK4	LK4 is connected so that $\overline{\text{SLEEP}}$ is tied to DVDD and, hence, the AD9831 is powered up.
LK5	REFOUT is tied to REFIN.
SW	All the SW switches are arranged so that DVDD is selected.

EVALUATION BOARD INTERFACING

Interfacing to the evaluation board is via a 36-way centronics female connector, J1. The pinout for the J1 connector is shown in Figure 1 and its pin designations are given in Table 2.

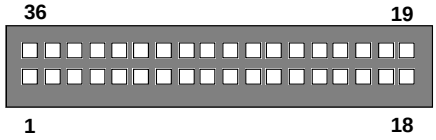


Figure 1. Pin Configuration for the 36-Way Connector, J1.

36-Way Connector Pin Description

DGND	Digital Ground. These lines are connected to the digital ground plane on the evaluation board.
DB0 - DB7	Data Bit 0 to Data Bit 7. Data transfers from the PC are 8 bits wide. Therefore, the 16 bit word is split into two 8 bit words. For each write operation, there are 3 transfers of data from the PC: the 8 MSBs of the 16 bit word, the 8 LSBs of the 16 bit word and the address data to bits A0, A1 and A2. The AD9831 accepts CMOS logic.
LOAD	When the 8 MSBs of the 16 bit word are written to the evaluation board from the PC, the word is held in a latch, a 74HC574 latch. This latch latches in the data on the rising edge of the CK signal. The LOAD signal provides this rising edge.
LATCH	The 8 LSBs of the 16 bit word are held in the latch U3. The rising CK edge to this part is provided by LATCH.
$\overline{\text{WR}}$	Write. This is an active low logic input which is used to write the digital data to the AD9831. When the address bits A0, A1 and A2 are being written to, the $\overline{\text{WR}}$ signal is generated also. On the rising edge of $\overline{\text{WR}}$, the AD9831 reads in the 16 bit word from the 74HC574 latches along with the address values.
$\overline{\text{RESET}}$	Reset. When $\overline{\text{RESET}}$ is taken low, the AD9831 is reset. On reset, the phase accumulator is reset to zero.

Table 2. 36-Way Connector Pin Funtions

PIN NO.	MNEMONIC
1	LATCH
2	D0
3	D1
4	D2
5	D3
6	D4
7	D5
8	D6
9	D7
14	$\overline{\text{RESET}}$
19	DGND
20	DGND
21	DGND
22	DGND
23	DGND
24	DGND
25	DGND
26	DGND
27	DGND
28	DGND
29	DGND
30	DGND
31	LOAD
36	$\overline{\text{WR}}$

Note: The remainder of the pins on the 36-way connector are no connects.

SOCKETS

There are six sockets relevant to the operation of the AD9831 on this evaluation board. The function of these sockets is outlined in Table 3.

Table 3. Socket Functions

Socket	Function
REFIN	Sub-Miniature BNC Socket for REFIN.
IOUT	Sub-Miniature BNC Socket for IOUT.
MCLK	Sub-Miniature BNC Socket for the MCLK input.
FSEL	Sub-Miniature BNC Socket for FSELECT.
PSEL0	Sub-Miniature BNC Socket for PSEL0.
PSEL1	Sub-Miniature BNC Socket for PSEL1.

CONNECTORS

There are three connectors on the AD9831 evaluation board as outlined in Table 4.

Table 4. Connector Functions

Connector	Functions
J1	36-Way Centronics Connector.
J2	PCB Mounting Terminal Block. The Digital Power Supply to the Evaluation Board is provided via this Connector.
J3	PCB Mounting Terminal Block. The Analog Power Supply to the Evaluation Board is provided via this Connector.

SWITCHES

There is one switch on the AD9831 evaluation board. This switch is a double throw, end stackable switch. This switch can be used to control the FSELECT, PSEL0 and PSEL1 inputs.

SOFTWARE DESCRIPTION

Included in the EVAL-AD9831EB evaluation board package is a PC-compatible disk which contains software for controlling the AD9831 using the printer port of a PC. The disk contains the executable program which runs under Windows and it is advised that the user copy this file to the system hard disk to obtain optimum performance from the software.

PC Configuration

The executable program contains two menus. The first menu gives options on the type of PC being used. The printer port needs to be configured correctly for one of the three different PC-types for interfacing to the AD9831. Choose the required printer type from the menu. The PC printer port is now configured for operation with the AD9831 evaluation board.

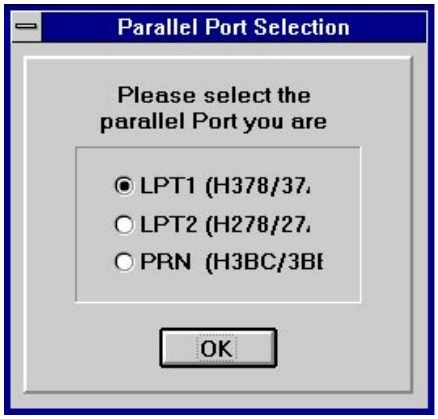


Figure 2. Parallel Port Selection

Running the AD9831 Software

The second menu gives options for running the AD9831. All registers of the AD9831 can be written to using this software. The MCLK frequency is set to 25 MHz by default in the program. However, the user has the capability of changing the MCLK frequency. When the master clock has a frequency other than 25 MHz, the user can change the value of the MCLK frequency in the program so that the software can correctly calculate the digital words corresponding to the different output frequencies.

The Frequency Registers are written to by writing in the required frequency in MHz to the PC. The AD9831 software will calculate the corresponding word which will be written to the AD9831 and display the word in hex on the screen. The Phase Registers are written to by writing in the required value in decimal to the PC. The software will then control the loading of this information into the AD9831.

To write to a Phase Register, three transfers of data from the PC are needed since the PC uses 8-bit transfers. The 16 bit word along with the address of the destination register is transferred from the PC to the AD9831. The sixteen bit word is split into two 8-bit words (the 8 MSBs and the 8 LSBs). The first transfer of data involves transferring the 8 MSBs of the 16-bit word. When these 8 bits are being transferred, a pulse is also generated on the LOAD pin so that the 8 bits of data are latched into U2 on the rising edge of LOAD.

During the second transfer, the 8 LSBs are transferred to U3, a pulse being generated on the LATCH pin so that these 8 bits are latched into U3.

The third transfer involves transferring the address of the destination register (A0, A1 and A2). When the PC outputs the address information (which is available on D0, D1 and D2 respectively), the PC also generates the $\overline{WR}$ pulse. On the rising edge of $\overline{WR}$, the 16 bits of data are read from the 74HC574 latches and the address of the destination register is read from the data bus.

Because the Frequency Registers are 32 bits wide, there will be six transfers from the PC when these registers are being written to. Writing the 16 LSBs to the Frequency Register involves transferring the destination register address (000 or 010) and the 16 bits of data. Similarly, the destination address for the 16 MSBs (001 or 011) and 16 bits of data need to be transferred when writing to the 16 MSBs of the Frequency Register.

The logic inputs FSELECT, PSEL0 and PSEL1 are not controlled by the PC. These inputs can be controlled using the switch SW or, alternatively, these inputs can be controlled using an external source via the BNC connectors.

The AD9831 software also contains a demonstration procedure whereby the AD9831 can be made to step through a series of output frequencies. The user only needs to load the start frequency, the stop frequency and the step size and, the AD9831 software will program the AD9831 appropriately so that a frequency sweep will be performed at the AD9831 output.

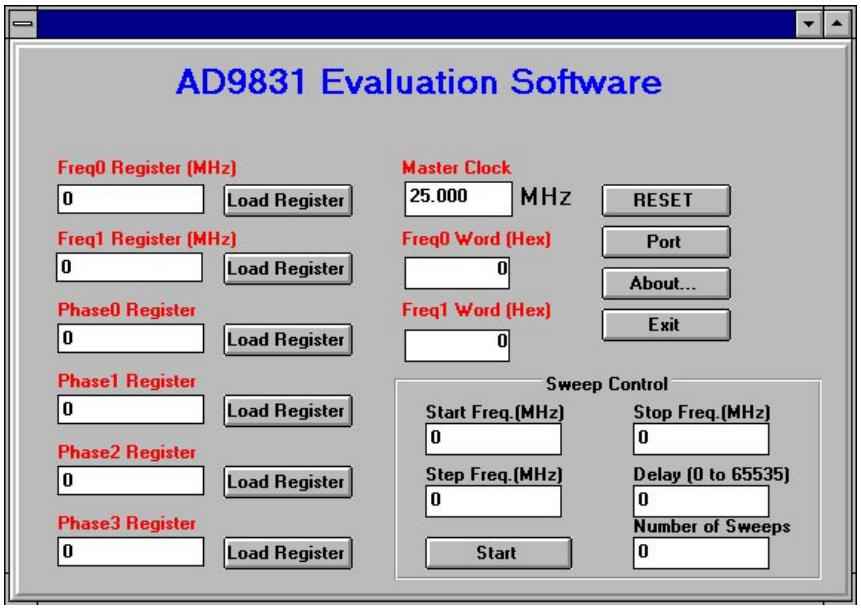
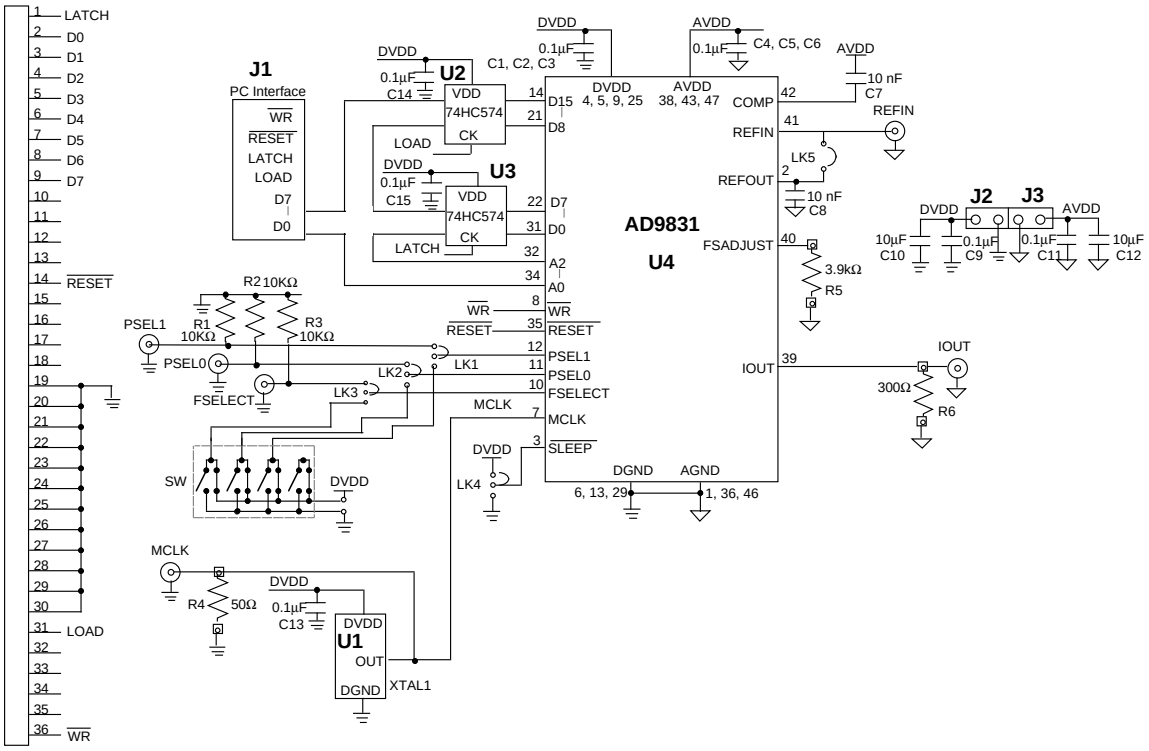


Figure 3. Main Menu



COMPONENT LIST

Integrated Circuits

XTAL1	OSC XTAL 25 MHz
U2, U3	74HC574 Latches
U4	AD9831 (48-Pin TQFP)

Capacitors

C1 - C6	0.1µF Ceramic Chip Capacitor
C7, C8	10nF Ceramic Capacitor
C9, C11, C13 - C15	0.1µF Ceramic Capacitor
C10, C12	10µF Tantalum Capacitor

Resistors

R1 - R3	10kΩ Resistor
R4	50Ω Resistor
R5	3.9kΩ Resistor
R6	300Ω Resistor

Links

LK1 - LK4	Three Pin Link
LK5	Two Pin Link

Switch

SW	End Stackable Switch (SDC Double Throw)

Sockets

MCLK, PSEL0, PSEL1, FSELECT, IOUT, REFIN	Sub-Miniature BNC Connector

Connectors

J1	36-Pin Edge Connector
J2, J3	PCB Mounting Terminal Block